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(54) IMPROVEMENTS RELATING TO SEQUENTIAL CONTROL SYSTEMS

(71) We, MACHINE TOOL INDUSTRY RESEARCH ASSOCIATION, a British Company of Hulley Road, Hurdsfield, Macclesfield, Cheshire, SK10 2NE, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a sequential control system and a method of generating a sequence of output signals for a control system.

Sequential controllers for machines or systems are required to generate a sequence of output signals in response to input signals, some of which may result from instructions given to the controller and some of which may indicate the current state of the machine or system. In the control of machine tools, for example, input signals of the first type are commonly-derived from switches or push-buttons whilst signals of the second type are obtained from limit switches. The output signals are used, after amplification if necessary to operate relays, contactors, valves etc. which control the operation of the machine. All the devices involved in sequential controllers are essentially two-state on-off devices and the input and output signals are combinations of binary digits, each indicating the actual or desired state of a particular input or output device.

A commonly used method of obtaining the output signals corresponding to any given combination of input signals is to pass the binary word representing the input signals through a series of interconnected logic gates which form the controller. Design of the controller, for example by the use of Boolean algebra, involves the establishment of the appropriate interconnections between the logic gates so as to give the correct set of output signals for each possible set of input signals, and is a time-consuming process. Moreover, when the controller has been designed and made it is specific to that particular control system.

It is desirable that the design and manufacture of sequence controllers for particular purposes should be made simpler by eliminating

(a) the need for the determination of a suitable control circuit, e.g. by the application of Boolean algebra;

(b) the necessity to wire up each controller separately according to the particular design developed in (a).

One way of simplifying the design of the logic system is to use a stepping switch (uniselector or an electronic equivalent) to select sequentially the required combination of output signals for each stage in the cycle of the machine or system to be controlled. On completion of one stage appropriate input signals selected by a simple system of logic gates cause the stepping switch to advance one step. However, it is possible for the stepping switch to become out of phase with the process thereby causing the process to miss one or more steps of the sequence. Electrical interference is likely to cause difficulties of this kind.

The realisation that a sequence controller can be considered as a memory unit which produces the desired output signals in response to the appropriate input signals has led to the development of sequence controllers using various types of memories. These memories are usually of the read-only type since it is not usually necessary to modify (or rewrite) the memory content once the correct sequence has been established.

One system known to use programmable read-only memories uses magnetic memory units of the type used in computers. The logic control circuit is designed and tested on an actual system to be controlled using conventional computer programming techniques in a normal computer. When the program is working satisfactorily a control system, incorporating read-only memories, is prepared from a copy of the computer program which was developed.

A second system, the programmable matrix controller, is known which uses the more recently introduced semi-conductor

programmable read-only memory units which can contain a large number of bits (binary digits) which can be set to the 0 or 1 state by a programming procedure. These programmable read-only memories are used to construct the logic control unit to develop the output states from the input states in the conventional way. After preparing a ladder diagram of switches such as is used in the older relay-type logic systems, e.g. by the use of Boolean algebra, the program is then developed from this using six computer-type instructions and the read-only memories are programmed accordingly.

According to one aspect of the present invention, there is provided a sequential control system for generating a sequence of output signals in response to a corresponding sequence of input signals comprising a first memory for storing at each of a plurality of storage locations information corresponding to one of the input signals, a second memory for storing at each one of corresponding storage locations, information defining an output signal corresponding to each of the input signals, a memory scanner for scanning in sequence, corresponding locations of both memories, a comparator for comparing a current existing input signal with the information stored in a location of the first memory currently being scanned, and, upon detecting coincidence between the current input signal and the information in the location of the first memory currently being scanned, feeding the output signal from the location of the second memory, corresponding to that of the first memory for which coincidence prevails.

According to another aspect of the present invention there is provided a method of generating a seqeunce of output signals in response to a corresponding sequence of input signals for a control system comprising the steps of feeding into a first memory at each of a plurality of storage locations information corresponding to one of the input signals feeding into a second memory at each one of corresponding storage locations information defining an output signal, corresponding to each of the input signals, scanning corresponding locations of both memories and comparing the current input signals derived from a process or machine being controlled with the information stored in a location of the first memory currently being scanned until coincidence is detected and feeding the output signal from the location of the second memory corresponding to that of the first memory for which coincidence prevails to the process or machine.

In order that the invention may be more clearly understood, one embodiment of the invention will now be described, by way of example with reference to the single figure of the accompanying drawing which shows a circuit diagram in block form of sequential control system.

Referring to this figure semiconductor read-only memories M1 and M2 are used to store all allowable combinations of the input signals (in M1) and corresponding required output signals (in M2). (The signal combinations would normally be stored in the order they occur in the sequence.). A pulse generator P and binary counter, BC, provide the means for addressing all the memory locations sequentially and extracting the stored information from each in turn. As each combination of input signals and the corresponding combination of output signals are addressed in turn they are fed out, in the case of the input signals to a comparator C and in the case of the output signals to the machine to be controlled. The pulse genetrator P is caused to run at a high frequency so that whilst the memories are being scanned each set of output signals in turn is fed to the machine for a time that is too short for them to have any effect.

The comparator C is used to detect when the particular combination of input signals addressed is identical with the actual combination of input signals at that instant as fed from the machine or system. When the comparator output indicates equivalence the gate G is inhibited, preventing further pulses from changing the binary count in BC. The stored input and corresponding output responses are then continuously available and the latter determine the operation of the machine.

Eventually, the output signals will cause the controlled process to change its state and provide a new set of input signals. Comparator C then releases control of gate G and sequential addressing continues until the new state is found in the memory.

The system could also be arranged so that output signals are fed to the machine or system to be controlled only when gate G is inhibited i.e. so that only the correct signals ever reach the machine.

The high-speed scanning of the memories renders the system virtually immune to interference from most sources of transient electrical noise. Transient electrical noise may cause the apparent input or output signals at any instant to differ from the true signals and may therefore result in incorrect output signals. With the system as described above, however, such incorrect output signals can appear only momentarily, if disturbed the system will cycle rapidly back to the correct state. Interference would become a problem only if the counter was regularly disturbed for a time during which the controlled process could respond.

Most controlled systems would normally follow one sequence, as described above, but alternative sequences (as might be required for emergency routines) could be added by

using switches (e.g. an emergency switch) to select alternative output memories (M3 etc.).

A system as described above has the additional advantages of easy programming from a knowledge of the required sequence and the one set of hardware will be suitable for a large range of different control systems by changing the memory units (the content of the input and output memories defines the actual sequence).

Thus the system consists of a sequential control system using memory elements to store information about all possible input signal states and also the output signal states corresponding to each of the input signal states. This avoids the need for the controller to generate the appropriate output signals from the corresponding input signals by means of interconnected logic elements using Boolean algebra or by computer programming techniques. A comparator is used to compare the current states of the input signals from the controlled system with the states stored in the memory locations and when a coincidence is detected the corresponding output control signal is provided from the memory locations to actuate the controlled system.

In order to select the appropriate memory locations a pulse generator is used with a logic gate and a binary counter to inspect all allowable input signal combinations in turn and, by generating a signal to inhibit further cycling, to stop when the combination corresponding to the current input signals from the machine or process is found. The frequency of the pulse generator can be so high (typically 4 M Hz or more) that the system can scan all possible states of the input variables in a time which is substantially less than the response time of any part of the controlled system. During the scanning all the output signals may be applied in turn to the system being controlled or it may be arranged that the output signals are provided only when the gate G is inhibited.

For each possible combination of input signals several possible alternative combinations of output signals can be provided, the choice between the possible combinations of output signals being made by one or more single binary signals. This allows alternative sequences of operation to be followed by the controlled system in the case of emergencies and the like.

Although read only memories are referred to above the memory units may be any form of memory such as could be used in digital computers, including by way of example magnetic core memories or semiconductor programmable read-only memories, the latter having the advantage of ease of programming.

WHAT WE CLAIM IS:—

1. A sequential control system for generating a sequence of output signals in response to a corresponding sequence of input signals comprising a first memory for storing at each of a plurality of storage locations information corresponding to one of the input signals, a second memory for storing at each one of corresponding storage locations, information defining an output signal corresponding to each of the input signals, a memory scanner for scanning in sequence, corresponding locations of both memories, a comparator for comparing a current existing input signal with the information stored in a location of the first memory currently being scanned, and, upon detecting coincidence between the current input signal and the information in the location of the first memory currently being scanned, feeding the output signal from the location of the second memory corresponding to that of the first memory for which coincidence prevails.

2. A sequential control system as claimed in Claim 1, wherein the memory scanner comprises a high frequency pulse generator.

3. A sequential control system as claimed in Claim 2, wherein the pulse generator has a frequency of 4 M Hz or more.

4. A sequential control system as claimed in Claim 2 or 3, wherein the pulse generator is used in conjunction with a logic gate and a binary counter and the logic gate is connected to the comparator and is inhibited to prevent further scanning when said coincidence is detected.

5. A sequential control system as claimed in Claim 4, wherein means are provided to ensure that output signals are provided only when the logic gate is inhibited.

6. A sequential control system as claimed in any preceding claim, wherein a further memory, is provided to store another choice of output signals corresponding in sequence to the input signals.

7. A sequential control system as claimed in Claim 6, wherein switch means are provided to switch from the second memory to the further memory.

8. A sequential control system as claimed in any preceding claim, wherein the memories are magnetic core memories.

9. A sequential control system as claimed in any of Claims 1 to 7 wherein the memories are semiconductor programmable read-only memories.

10. A sequential control system for generating a sequence of output signals in response to a corresponding sequence of input signals substantially as hereinbefore described with reference to the accompanying drawing.

11. A method of generating a sequence of output signals in response to a corresponding sequence of input signals for a control system comprising the steps of feeding

into a first memory at each of a plurality of storage locations information corresponding to one of the input signals feeding into a second memory at each one of corresponding storage locations information defining an output signal, corresponding to each of the input signals, scanning corresponding locations of both memories and comparing the current input signals derived from a process or machine being controlled with the information stored in a location of the first memory currently being scanned until coincidence is detected and feeding the output signal from the location of the second memory corresponding to that of the first memory for which coincidence prevails to the process or machine.

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1 SHEET *This drawing is a reproduction of the Original on a reduced scale*